REMARKS

Claims 1-17 are pending. Claims 14-16 were canceled and claim 17 is new. Claims 1-16 were rejected under 35 U.S.C. 102(b) as being anticipated by Noda (5,784,119). Claims 1-16 were rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (6,288,748).

Watanabe describes a system for creating video information in which changes in the number of scanning lines per filed appear at random. This has the objective of providing a display capable of satisfactory suppression of vertical jitter, even when displaying video information in which changes in the number of scanning lines per field appear at random (column 2, lines 15-25).

Noda describes a system for decoding video data in synchronism with a system clock and thereby obviating frame slipping and other errors. A video decoding section decodes, in response to the first clock, the video data included in the multiplex data. A second clock generating section generates a second clock for video display and synchronous to the first lock. A video data outputting section outputs, in response to the second clock, the video data decoded by the decoding section (column 1, lines 43-55).

However, neither of the references teach or suggest qualified system time events or derived time events. The independent claims 1, 8, 9, and 14 recite qualified system time events and derived time events. Claim 1 recites "receiving said qualified system time events and converting said qualified system time events to one or more derived time events." Claim 8 recites "decoding said SYNC stream into a plurality of qualified system time events" and creating and synchronizing derived time events contained in said qualified system time events packets." Claim 9 recites "converting of said qualified system time events by said SYNC receivers to one or more derived time events."

The material cited by the Examiner in Noda only mentions a system decoding block 13. The system decoding block 13 "detects, based on the result of analysis of the header information, the timing at which the last byte of an SCR (System Clock Reference)/PCR (Program Clock Reference) field included in the multiplex data arrives, generates a counter load timing signal LD on the basis of the result of detection, and delivers the signal LD to the STC counting 14"

(column 3, lines 25-30). However, Noda does not teach or suggest "converting said qualified system time events to one or more derived time events" as recited in the claims.

The material cited by the Examiner in Watanabe only mentions a "system clock generator for generating a main clock pulse for the decoder 110" (column 6, lines 23-25). However, Watanabe does not teach or suggest converting said qualified system time events to one or more derived time events" as recited in the claims.

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 778
Berkeley, CA 94704-0778
(510) 843-6200